Focus Group on Quantum Technologies

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ABSTRACT

In this contribution we propose definitions for commonly used terminology that applies to solid-state, gate-based quantum computing. The purpose of it is to achieve a consistent terminology on these matters. This contribution is intended as a literal text proposal for inclusion into „Annex X: Solid-state Quantum Computing". (see N058a) For the time being we refer to it as annex „X", but that should be replaced by the appropriated number when the Roadmap Editor has updated the draft.

Explanation of changes

Provide a first proposal for terminology.

Why are the changes needed?

There is currently no agreed-upon definition of what operations, gates and pulses are, which is required to describe them and what they act on. However, these terms are commonly used and have extensive implied meaning.

X.2 Terminology

X.2.1 Definitions

For the purposes of the present document, the following terms and definitions apply:

Schedule

A Schedule is a data structure which includes Operation(s) and the information about when and where to apply the Operation to.

Operation

An operation describes an action to be applied/performed on a resource(s). Examples of operations are gates and measurements as well as control pulses.

Resource

A resource is something on which an operation acts. It can be viewed as the location where an Operation is applied to. Examples are qubits, ports and clocks.

Quantum-circuit level

The Quantum-circuit level description is an idealized mathematical description of operations (such as gates and measurements) acting on qubits that is commonly used to describe quantum algorithms.

Quantum-device level

The quantum-device level description is a quantum device specific description that specifies the (electrical) signals to be applied to a chip and how to interpret signals coming from a chip.

Hardware-instructions level

The hardware-instructions level description is a control electronics specific description that specifies the instructions to be executed in hardware.

Editorial note: Qubits, gates and measurements are described here. In the representation context, we currently only describe ideal qubits, gates and measurements. We propose to add noisy qubits subject to decoherence and gate errors, and generalizations such as qutrits and/or qudits in a later contribution.

Qubit

The definition of a qubit is context dependent.

In a **programmatical context** it refers to a calculation element for storing and manipulating a pair of arbitrary complex numbers, α and β with the restriction that $|\alpha|^2+|\beta|^2=1$. The linear algebra way of expressing the contents of a qubit is a column vector with two elements $|\psi\rangle=[\alpha,\beta]$, where the restriction is expressed as: norm($|\psi\rangle$)=1. Note that in the programmatical context, the coefficients α and β are not directly accesible.

In an **ideal representation context** a qubit is a two-level quantum-mechanical system. The state of a qubit can be represented by the state vector $|\psi\rangle=\alpha|0\rangle+\beta|1\rangle$, where α and β are complex valued coefficients with norm: $|\alpha|^2+|\beta|^2=1$.

In an **implementation context** a qubit refers to a physical system that can be represented as a two-level quantum-mechanical system, can be initialized in a well defined state, can be manipulated using a universal set of quantum gates, has a coherence time significantly longer than the duration of the gates, and can be measured. Examples of qubits are superconducting transmon qubits, spin qubits, trapped ions, etc.

A qubit is a resource.

Gate

The definition of a gate is context dependent.

In a **programmatical context** it refers to an arithmatic operation on the contents of one or more qubits. The linear algebra way of expressing this operation is a matrix multiplication $|\psi_2\rangle=U|\psi_1\rangle$, where U is a $2n\times2n$ a $2n\times1$ column vector representing the content of the qubits.

In an **ideal representation context** a gate is an operation that can act on qubits. A gate U which acts on n qubits can be described by a $2n\times2n$ unitary matrix acting on the state $|\psi\rangle$ of the qubits. The action of the gate U on a specific quantum state $|\psi_1\rangle$ is found by multiplying the $2n\times1$ vector $|\psi_1\rangle$ which represents the state, by the matrix U representing the gate. The result is a new quantum state $|\psi_2\rangle$:

In an **implementation context** a gate refers to the control signals used to manipulate the state of a qubit.

A gate is an operation.

Measurement

The definition of a measurement is context dependent.

In a **programmatical** context, a measurement is a logical operation on the contents of one or more qubits that verifies if the qubits are in a specified state and returns the qubits in the measured state and classical bits corresponding to the measured state.

In an **ideal representation context** a measurement is an operation that projects one or more qubits into an eigenstate of the measurement operator and returns the corresponding eigenvalue as a classical value. The state of the system after the measurement corresponds to the eigenstate the system was projected into. The probability of projecting into an eigenstate is given by the inner product of the eigenstate of the measurement operator and the state of the system. A measurement on one or more qubits can be described by a positive operator-valued measure (POVM).

In an **implmentation context** a measurement refers to the control signals used to probe the qubits and the data acquisition required to interpret the resulting signal.

A measurement is an operation.

Measurement in the computational basis

A measurement of a qubit in the computational basis measures

the $Z = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}$ operator whose eigenvectors are $|0\rangle$ and $|1\rangle$ with eigenvalues +1 and −1. These eigenvalues are commonly mapped to the Boolean values of $+1 \rightarrow \mathit{False} = 0$, and $-1 \rightarrow \mathit{True} = 1$ to correspond to the measured state of the qubit.

Gate-schedule

A gate schedule specifies the order in which operations are applied as well as any conditionality of operations on other operations. A graphical way of expressing a gate-schedule is a circuit diagram. A gate-schedule is a schedule.

Pulse-schedule

A pulse-schedule specifies the timing constraints between operations as well as any conditionality of operations on other operations. A pulse-schedule is a schedule.

Editorial note: Because specifying when operations occur in time also specifies the order, a pulse-schedule is also a valid gate-schedule.

Port

A port is a physical location on a device that a signal can be applied to. An example of a port can be the end of a flux-bias line used to control a transmon qubit. A port is a resource.

Reference clock

A reference clock specifies the frequency and phase with which to apply a signal. A reference clock is typically set up to track/correspond to a physical transition, but this is not required. An example of a reference clock is a reference clock that tracks the ge transition of a transmon qubit. A baseband pulse can be specified by using a reference clock with frequency set to 0. A reference clock can be used to modulate a control pulse. A reference clock is a resource.

Control pulse

A control pulse specifies a complex valued waveform as a function of time that is applied to a port using a specific clock. In the case of modulation, the real-component of the waveform corresponds to the in-phase or I component and the imaginary component of the waveform corresponds to the out-of-phase or Q component of the waveform. When no modulation is used, the pulse should be real-valued i.e., the imaginary component is zero. This description is allowed to be a parameterized function. A control pulse is part of an operation.

Acquisition protocol

An acquisition protocol specifies how to interpret an acquired signal. An example of an acquisition protocol is weighted integration.

Weighted integration

Weighted integration is a method to reduce a complex valued signal $S(t)$ as a function of time to a single complex number $Z=I+1jQ$. In weighted integration, acquisition weights $WI(t)$ and $WQ(t)$ are multiplied with an acquired signal and then integrated over time resulting in a complex number:

$$I=\int(\mathrm{Re}(S(t))\cdot\mathrm{Re}(WI(t))+\mathrm{Im}(S(t))\cdot\mathrm{Im}(WI(t)))dt$$

$$Q=\int(\mathrm{Re}(S(t))\cdot\mathrm{Re}(WQ(t))+\mathrm{Im}(S(t))\cdot\mathrm{Im}(WQ(t)))dt$$

Acquisition weights

Acquisition weights specify a complex-valued waveform as a function of time that can be used to interpret acquired signals using weighted integration. Acquisition weights are part of an operation.

Composite Pulse

A composite pulse can contain one or more control pulses and or acquisition weights. A composite pulse is an operation.

Interface

A point where two systems, subjects, organizations, etc. meet and interact. Different compilation steps are required to go from a high-level description of a quantum algorithm to something that can be executed on hardware. The interface description specifies the allowed operations, and how to translate these between the layers.

Quantum-circuit level interface

The quantum-circuit level interface exposes to a higher-level what operations are allowed to be at the quantum-circuit level. This interface specifies what operations are allowed and on which qubits they can act. The quantum-circuit level interface can be specified in terms of a gate set.

Gate set

A gate set specifies the allowed gates and measurements supported at the quantum-circuit level. The gate set should contain information on what qubits these operations can be performed on.

Editorial note: A gate set does not have to be discrete, thus allowing parameterized gates.

Editorial note: By specifying on which qubits operations can be performed, the connectivity is implicitly specified in the gate set.

Circuit-to-device level interface

The circuit-to-device level interface exposes the quantum-device level description to the quantum-circuit level description. The circuit-to-device level interface should describe which operations at the quantum-circuit level are supported and can be translated to the quantum-device level description. The circuit-to-device level interface should describe how to translate the quantum-circuit level description to the quantum-device level description. To do this, the circuit-to-device-level interface should at least describe how to translate gates and measurements on qubits to

control pulses and acquisition protocols on ports and clocks. A specification of this configuration is out of scope for this submission.

Device-to-instruction level interface

The device-to-instruction level interface exposes the hardware-level description to the quantum-device-level description. The Device-to-instruction level interface should describe which operations at the quantum-device level are supported and can be translated to the hardware-instruction level. The device-to-instruction level interface should describe how to translate the quantum-device-level description to the hardware-instruction level description. A specification of this configuration is out of scope for this submission.

X.2.2 Abbreviations

For the purposes of the present document, the following abbreviations apply:

No abbreviations yet.